22C:060: Computer Organization
Spring 2010
Assignment 5

Total points = 50

Due April 15, 2010, 11:59:59 PM

Question 1. (20 points) Show how to connect four (16M x 1 bit) RAM modules to design a (64M x 1 bit) memory. A *clean diagram* is essential. Briefly explain how your design will work.

Question 2. (10 points) Consider a computer system with a 1 GB RAM. It uses a two-level cache: a 64 KB L1 cache with access time 1ns, and a 1 MB L2 cache with an access time of 2 ns. The L1 cache has a hit ratio of 90% and the L2 cache has a hit ratio of 80%. The miss penalty of the L2 cache is 100 ns. Calculate the average memory access time. Show your calculations.

Question 3. (20 points) Consider a system with a ***direct-mapped cache*** of size 128 (= 2^7) bytes, and a main memory of size of 1 KB (i.e. 1024 or 2^{10} bytes). Each cache line contains 8 bytes. A program running on the system accesses the following locations in the first ten steps:

1 10 1010 0100,
2 10 1010 1000,
3 10 1010 0100,
4 01 0000 0000,
5 00 1010 0000,
6 00 1010 1100,
7 00 1010 0100,
8 01 0000 0000,
9 10 1010 0000,
10 01 0000 0000

Assuming that the initial values of the cache tags and the cache lines are completely arbitrary, show which accesses will lead to a hit, and which will cause to a miss. Also, show how the cache tags will change for each of the above steps. You should justify your answer.