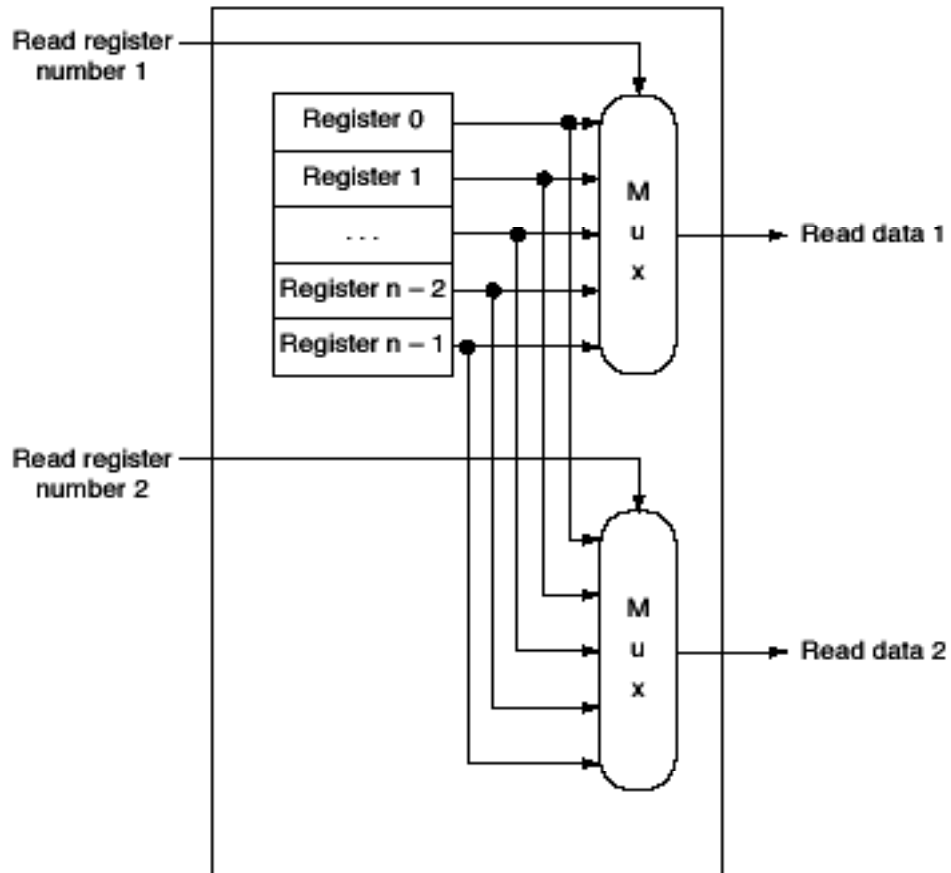
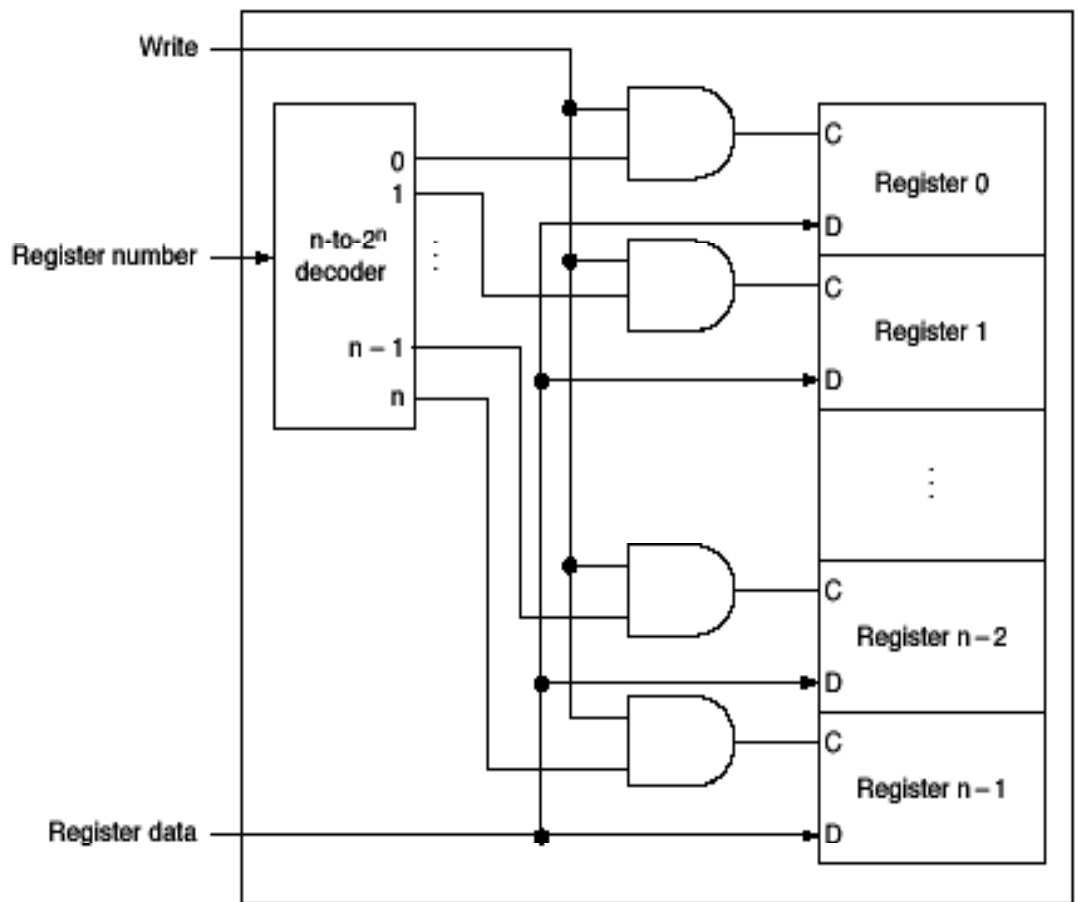


# Register file construction



**FIGURE B.8.8** The implementation of two read ports for a register file with  $n$  registers can be done with a pair of  $n$ -to-1 multiplexers each 32 bits wide. The register read number signal is used as the multiplexor selector signal. Figure B.8.9 shows how the write port is implemented.

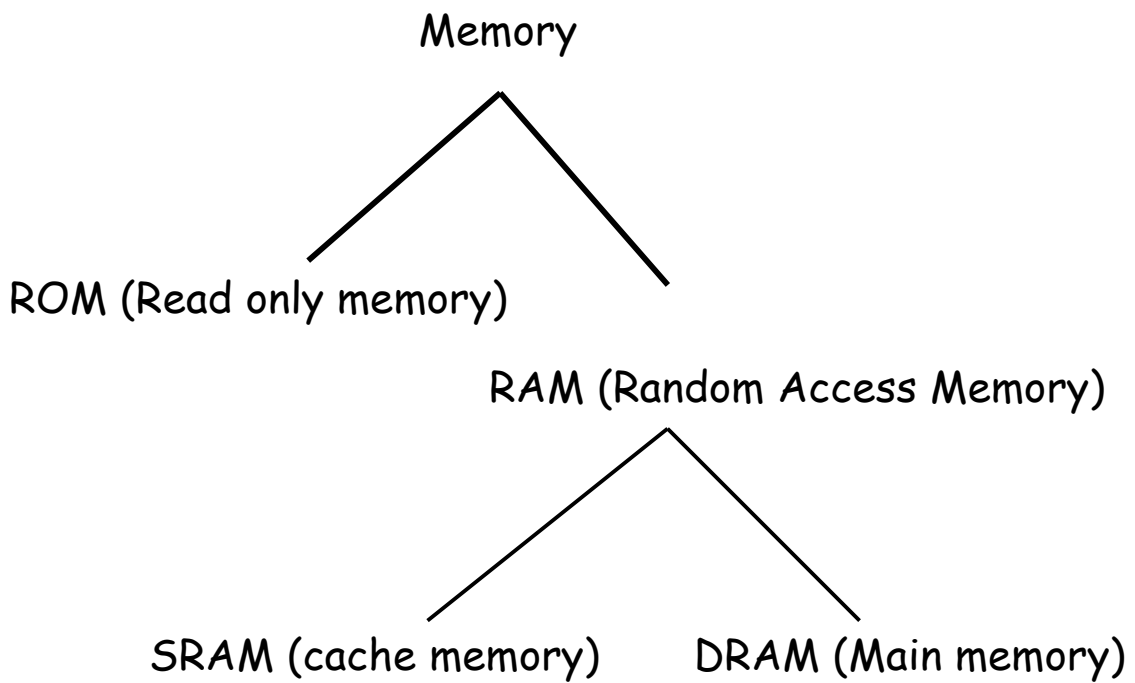
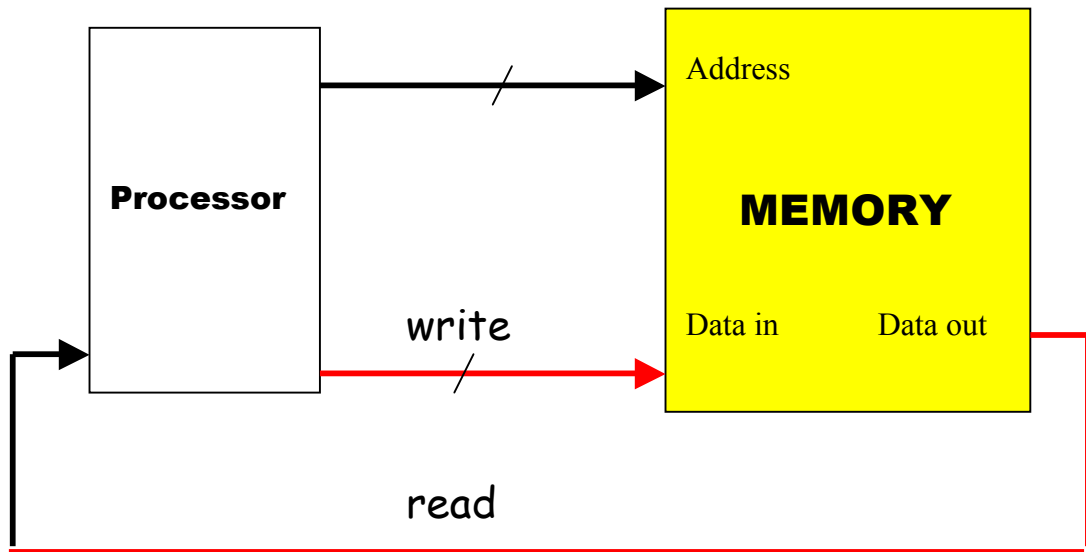
## Creating read ports



**FIGURE B.8.9** The write port for a register file is implemented with a decoder that is used with the write signal to generate the C input to the registers. All three inputs (the register number, the data, and the write signal) will have set-up and hold-time constraints that ensure that the correct data is written into the register file.

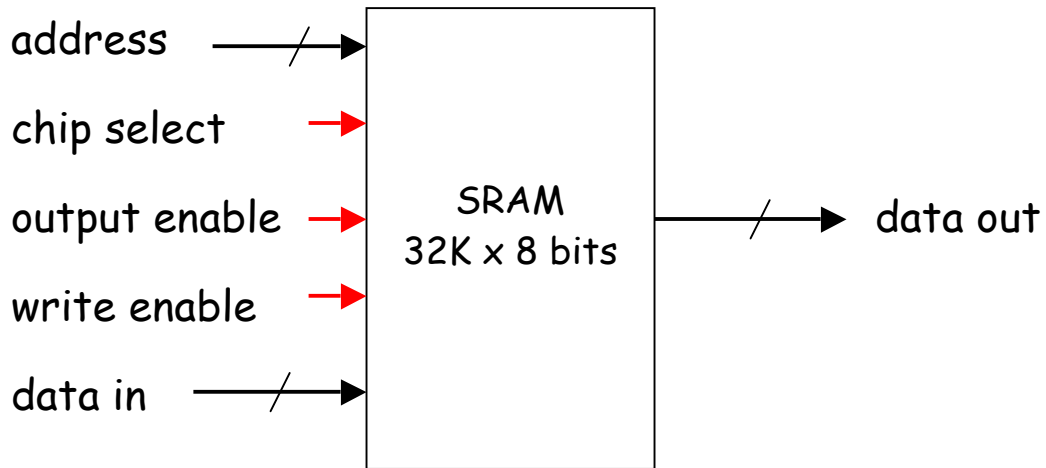
## Creating write port

## Main Memory

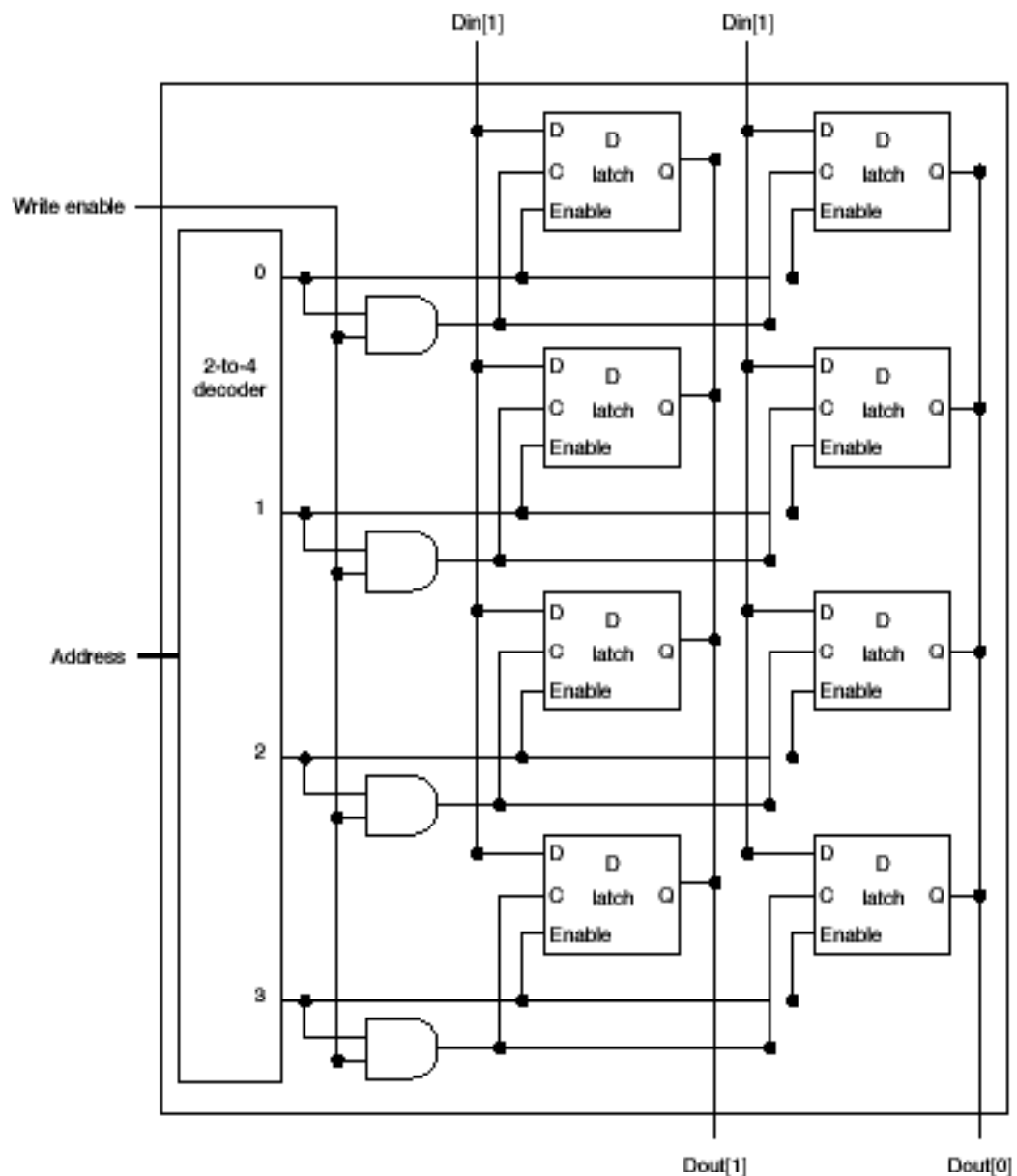


Typical sizes of SRAM are

(32 or 64 or 128 or 256) x (1 or 2 or 4 or 8 bits)

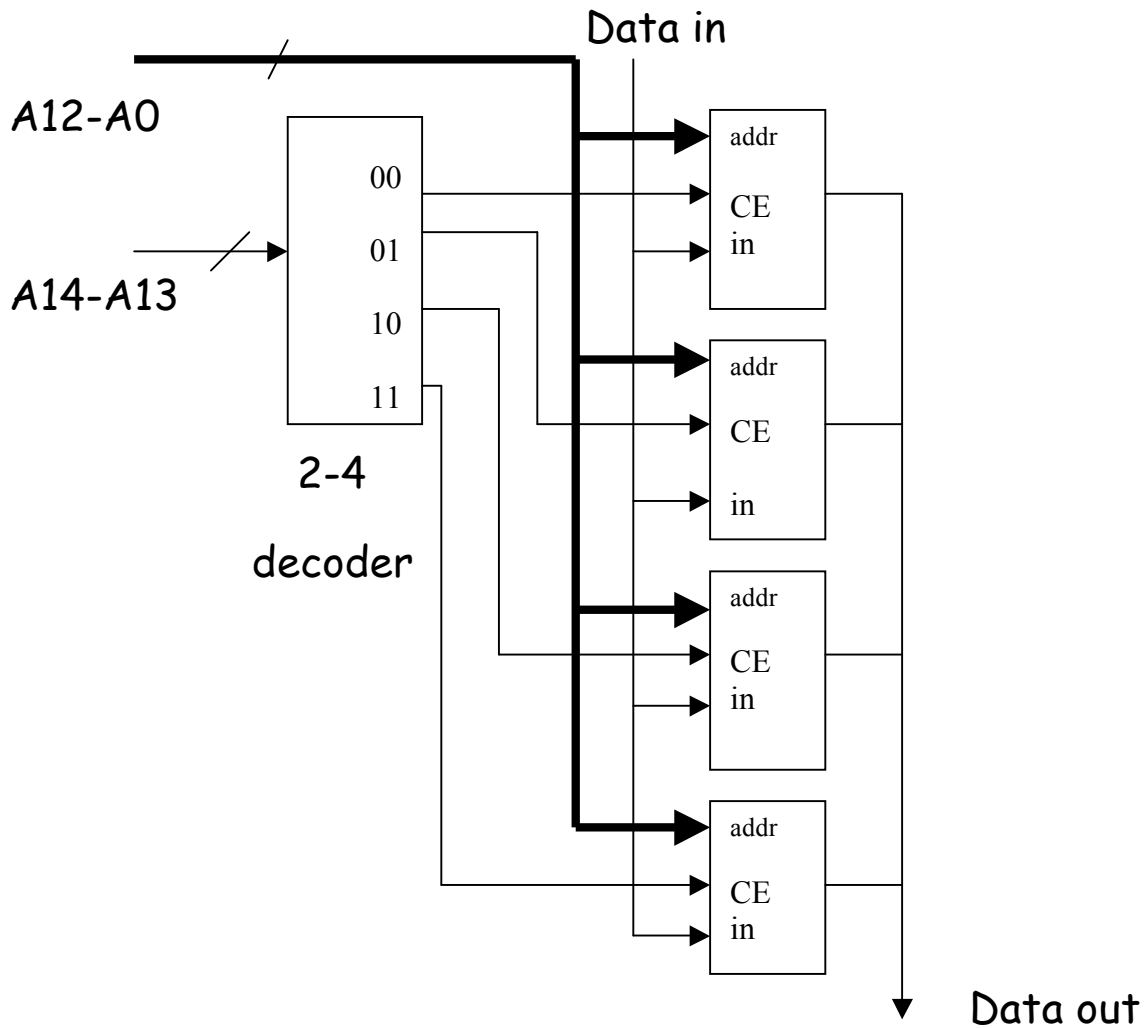


How many lines are there in **address**, **data in** and **data out**?



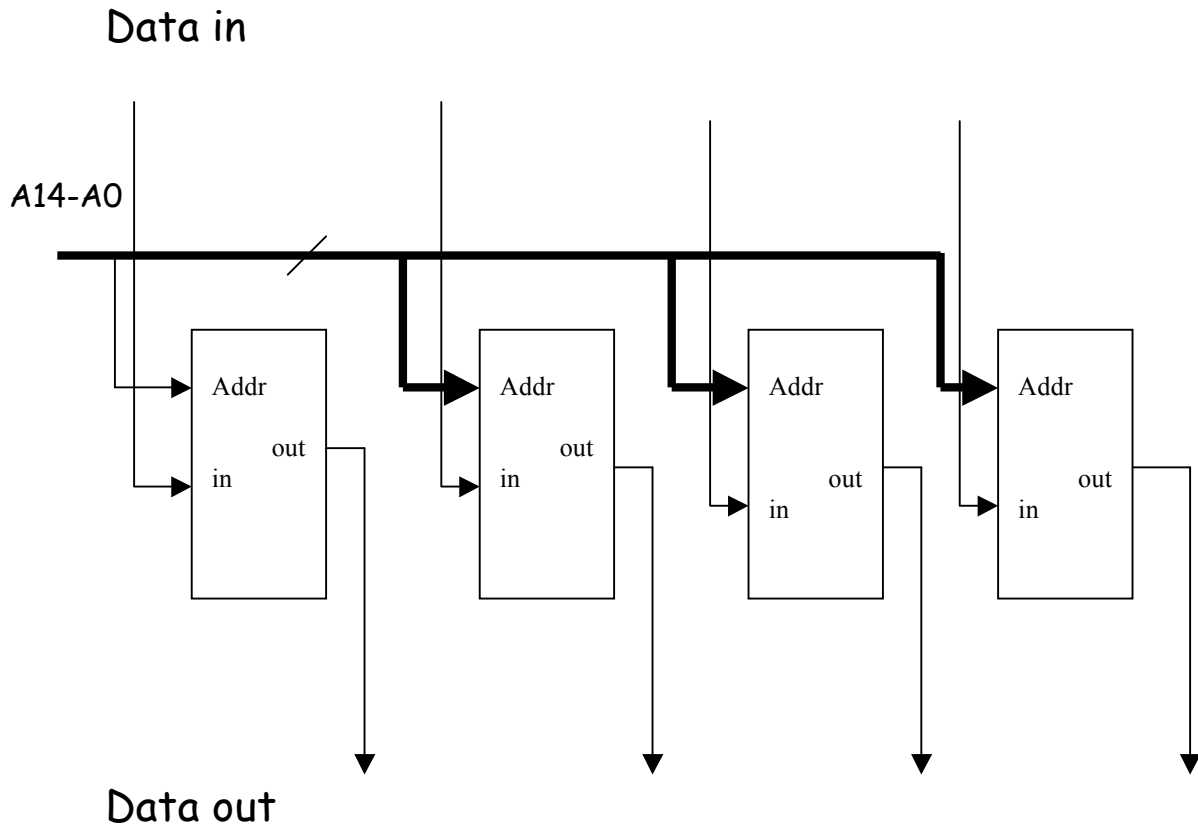
**FIGURE B.9.3** The basic structure of a  $4 \times 2$  SRAM consists of a decoder that selects which pair of cells to activate. The activated cells use a three-state output connected to the vertical bit lines that supply the requested data. The address that selects the cell is sent on one of a set of horizontal address lines, called the word lines. For simplicity, the Output enable and Chip select signals have been omitted, but they could easily be added with a few AND gates.

## 32K x 1 bit RAM using 4 8K x 1 RAMs



For each chip, the write enable line is set to 1 during a write operation, and the output enable lines are set to 1 during a read operation.

## 32Kx 4 bit RAM using 32K x 1 bit RAMs



For each chip, the write enable line is set to 1 during a write operation, and the output enable lines are set to 1 during a read operation.