Floating point operations in MIPS

32 separate single precision FP registers in MIPS
  f0, f1, f2, … f31,
Can also be used as 16 double precision registers
  f0, f2, f4, f30

These reside in a coprocessor in the same package

Operations supported

add.s   $f2, $f4, $f6   # f2 = f4 + f6 (single precision)
add.d   $f2, $f4, $f6   # f2 = f4 + f6 (double precision)

(Also subtract, multiply, divide format are similar)

lwc1    $f1, 100($s2)   # f1 = M [s2 + 100]  (32-bit load)

mtc1    $t0, $f0        # f0 = t0 (move to coprocessor 1)

mfc1    $t1, $f1        # t1 = f1 (move from coprocessor 1)
Sample program

Evaluation of a Polynomial \(a.x^2 + b.x + c\)

```plaintext
# $f0 --- x
# $f2 --- sum of terms

# Evaluate the quadratic
l.s     $f2,a           # sum = a
mul.s   $f2,$f2,$f0     # sum = ax

l.s     $f4,bb         # get b
add.s   $f2,$f2,$f4     # sum = ax + b
mul.s   $f2,$f2,$f0     # sum = (ax+b)x = ax^2 + bx

l.s     $f4,c          # get c
add.s   $f2,$f2,$f4     # sum = ax^2 + bx + c

.data
a:      .float  1.0
b:      .float  1.0
c:      .float  1.0
```
Design of registers

A 32-bit register is an array of 32 flip-flops. A flip-flop contains 1-2 latches inside it.

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0/1</td>
<td>1/0</td>
<td>Old state continues</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Set state</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Reset state</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Illegal inputs</td>
</tr>
</tbody>
</table>
A clocked D-latch

Clock is the enabler. If $C=0$, $Q$ remains unchanged. When $C=1$, then $Q$ acquires the value of $D$. We will use it as a building block of sequential circuits.

The main complaint is the "transparency". A master-slave circuit or an edge-triggered circuit (?) solves this problem (to be discussed in the class).
A Master-Slave D flip-flop

The output Q acquires the value of D, only when one complete pulse (i.e. 0 1 0) is applied to the clock input. The external output Q changes after the falling edge.

A clock pulse

rising edge  falling edge