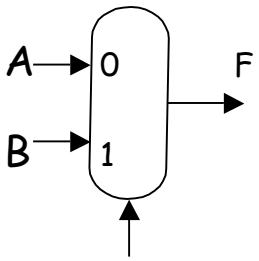
Multiplexor

It is a **many-to-one switch**, also called a **selector**.



Control S

S = 0, F = A
S = 1, F = B

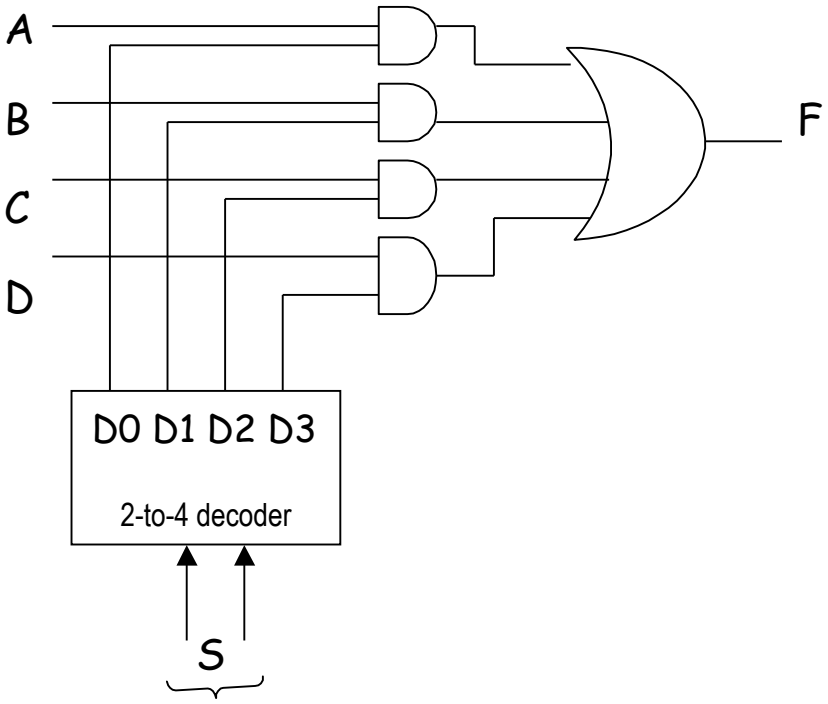
Specifications of the mux

A 2-to-1 mux

$$F = \overline{S}.\ A + S.\ B$$

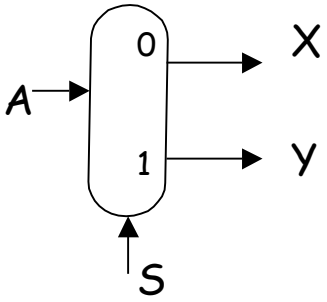
Exercise. Design a 4-to-1 mux.

Another design of a multiplexor



Demultiplexors

A demux is a one-to-many switch.



S = 0, X = A

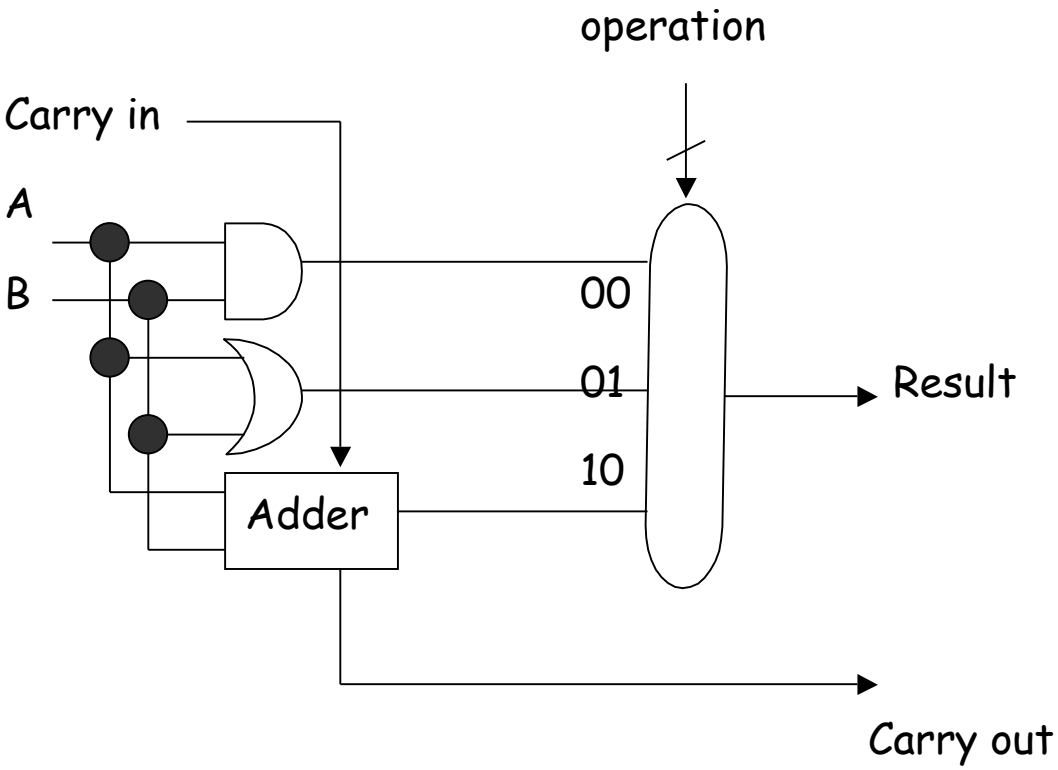
S = 1, Y = B

A 1-to-2 demux, and its specification.

So, $X = \overline{S}.A$, and $Y = S.B$

Exercise. Design a 1-4 demux.

A 1-bit ALU



Understand how this circuit works.

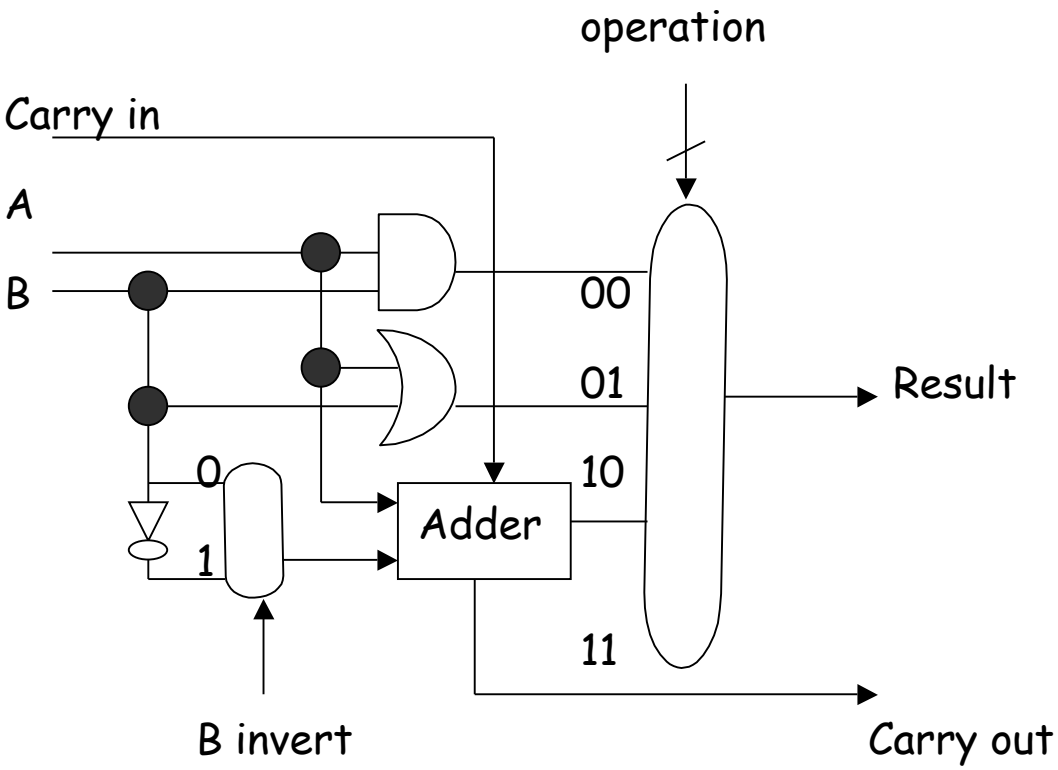
Need to add one more input to the mux to implement **slt**

Converting an adder into a subtractor

A - B (here - means arithmetic subtraction)

= A + 2's complement of B

= A + 1's complement of B + 1

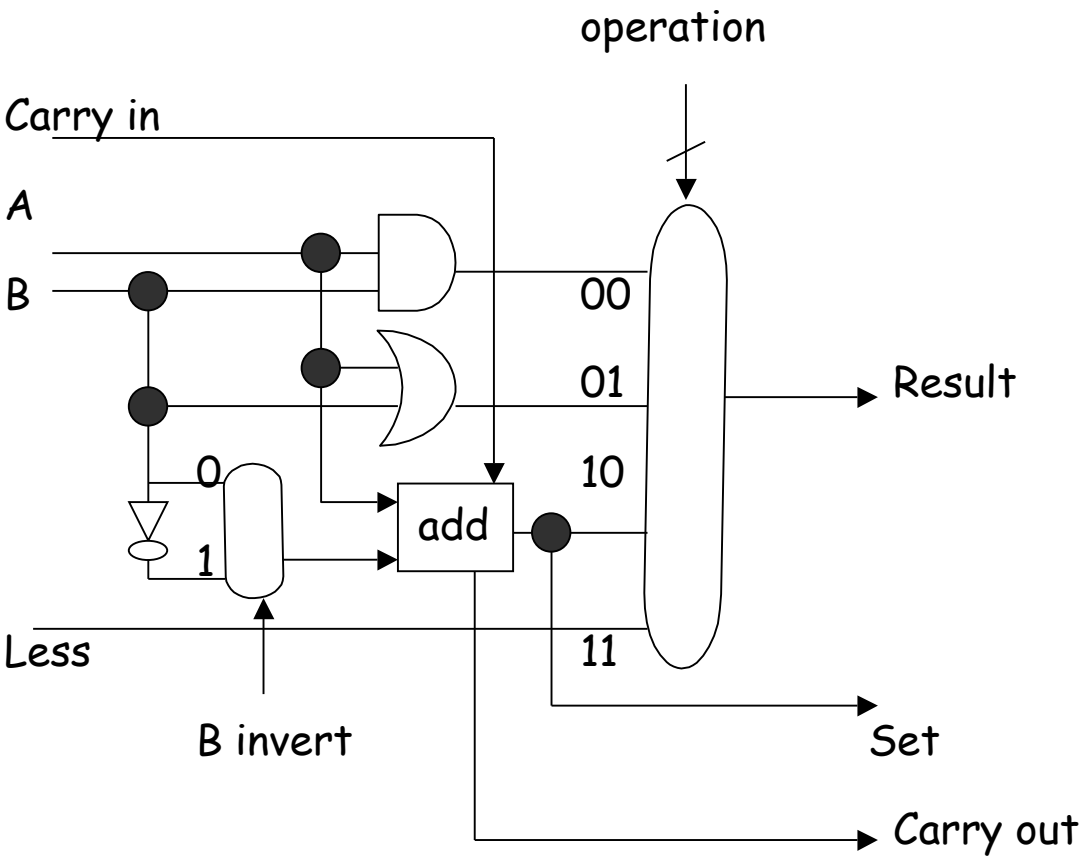


1-bit adder/subtractor

For subtraction, B invert = 1 and Carry in = 1

1-bit ALU for MIPS

Assume that it has the instructions add, sub, and, or, slt.



Less will be used to detect if the 32-bit number A is less than the 32-bit number B.

We now implement **slt** (If A < B then Set = 1 else Set = 0)

A 32-bit ALU for MIPS