Run time environment of a MIPS program

- Stack pointer
- Frame pointer
- Temporary local variables
- Return address
- Saved argument registers beyond a0-a3

Growth of stack

Low address

High address
A translation hierarchy

HLL program

COMPILER

Assembly language program

ASSEMBLER

Machine language module

LINKER ← Library routine

Executable machine language program

LOADER

Memory
What are Assembler directives?

Instructions that are not executed, but they tell the assembler about how to interpret something. Here are some examples:

```
.text
{Program instructions here}

.data
{Data begins here}
.byte 84, 104, 101
.ascii "The quick brown fox"
.float f1, , fn
.word w1, , wn
```
How does an assembler work?

In a two-pass assembler

PASS 1: Symbol table generation
PASS 2: Code generation

To be explained in the class ...
Other architectures

Not all processors are like MIPS.

Example. Accumulator-based machines

A single register, called the **accumulator**, stores the operand before the operation, and stores the result after the operation.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load x</td>
<td># into acc from memory</td>
</tr>
<tr>
<td>Add y</td>
<td># add y from memory to the acc</td>
</tr>
<tr>
<td>Store z</td>
<td># store acc to memory as z</td>
</tr>
</tbody>
</table>

Can we have an instruction

```
add z, x, y  # z:= x + y, (x, y, z in memory)
```

For some machines, YES, not in MIPS
Load-store machines

MIPS is a load-store architecture. Only load and store instructions access the memory, all other instructions use registers as operands. What is the motivation?

Register access is much faster than memory access, so the program will run faster.

Reduced Instruction Set Computers (RISC)

• The instruction set has only a small number of frequently used instructions. This lowers processor cost, without much impact on performance.
• All instructions have the same length.
• Load-store architecture.

Non-RISC machines are called CISC (Complex Instruction Set Computer). Example: Pentium
Another classification

3-address  add r1, r2, r3  \((r1 \leftarrow r2 + r3)\)

2-address  add r1, r2  \((r1 \leftarrow r1 + r2)\)

1-address  add r1  (to the accumulator)

0-address or stack machines  (see below)

Example of stack architecture

Push x
Push y
Push z
Add
Multiply
Pop z

Computes \(z = x \times (y + z)\)
Computer Arithmetic

How to represent negative integers? The most widely used convention is 2’s complement representation.

<table>
<thead>
<tr>
<th>+14</th>
<th>0,1110</th>
</tr>
</thead>
<tbody>
<tr>
<td>-14</td>
<td>1,0010</td>
</tr>
</tbody>
</table>

Largest integer represented using n-bits is $+2^{n-1} - 1$

Smallest integer represented using n-bits is $-2^{n-1}$

Review binary-to decimal and binary-to-hex conversions.

Review BCD (Binary Coded Decimal) and ASCII codes.

How to represent fractions?
**Overflow**

\[\begin{align*}
+12 & = 0,1100 \\
+2 & = 0,0010 \\
\text{add} & = 0,1110 \\
+14 & = 0,1110 \\
\text{add} & = \ ? \\
+12 & = 0,1100 \\
+7 & = 0,0111 \\
\text{add} & = 0,0111 \\
+14 & = 0,1110 \\
\text{add} & = 1,0011
\end{align*}\]

Addition of a positive and a negative number does not lead to overflow. *How to detect overflow?*
Exceptions

MIPS coprocessor has a cause register that contains a 4-bit code to identify the cause of an exception.

<table>
<thead>
<tr>
<th>Cause register</th>
<th>pending interrupt</th>
<th>exception code</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-10</td>
<td>5-2</td>
<td></td>
</tr>
</tbody>
</table>

MIPS instructions that cause overflow (or some other violation) lead to an exception (also called an interrupt), and transfer control to a predefined address to invoke a routine (exception handler) for handling the exception.

L: add $t0, $t1, $t2
  overflow!

Return address (L+4) is saved in EPC

Next instruction

Exceptions cause unscheduled procedure calls.
The following sequence of MIPS instructions can detect overflow in signed addition of $t1 and $t2:

```
addu $t0, $t1, $t2  # add unsigned
xor  $t3, $t1, $t2  # check if signs differ
slt  $t3, $t3, $zero  # $t3=1 if signs differ
bne  $t3 $zero, no_overflow
xor  $t3, $t0, $t1  # sum sign = operand sign?
slt  $t3, $t3, $zero  # if not, then $t3=1
bne  $t3, $zero, overflow

no_overflow:
...
...
overflow:
<Do something to handle overflow>
```
More Programming Examples

Copying a string

Each char is represented by an ASCII byte. The string is terminated by a **Null** in ASCII). Reg $s0 will hold the array index.

```assembly
add $s0, $zero, $zero  # i = 0

L1:  add $t1, $a1, $s0  # address of y[i] in t1
    lb $t2, 0($t1)  # t2 = y[i]
    add $t3, $a0, $s0  # address of x[i] in t3
    sb $t2, 0($t3)  # x[i] = y[i]
    addi $s0, $s0, 1  # i = i+1
    bne $t2, $zero, L1  # if y[i]=0 then goto L1
```