minute paper

1. One takeaway from last lecture
2. One question remaining from last week
CS 2630
Computer Organization

Meeting 23: Pipelining
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Let’s engineer a simpler function first

• Suppose we are building a robot that keeps track of the total distance it has traveled on the floor (2D)
• Every clock cycle, it receives inputs X and Y telling it how far to move in each dimension
three designs for Distance Counter

\[ soFar_{i+1} = soFar_i + x + y \]

- **single-cycle**
- **pipelined**
- **multi-cycle**

(see handout)
Pipelining

• (demo)
Administrivia

• Reminder: Project 2-1 due Nov 11, 11:59pm
• Project 2-2 will be a 2-stage pipelined MIPS processor
Pipelining

Original circuit

2-stage pipeline version
(break the combinational logic into two halves)
Let’s review the steps of how `lw` gets executed

[Diagram of the execution process of an `lw` instruction]

http://courses.cs.washington.edu/courses/cse378
IF: Instruction Fetch

read Instruction out of the instruction memory

http://courses.cs.washington.edu/courses/cse378
ID: Instruction Decode

read values from register file
EX: Execute

ALU computes a result

http://courses.cs.washington.edu/courses/cse378
MEM: Access memory

Read the data memory

http://courses.cs.washington.edu/courses/cse378
WB: Write back

Write the data back to register file
Peer instruction

• Match the stages to what happens in them during the branch instruction

1. IF
2. ID
3. EX
4. MEM
5. WB

a) compare two operands
b) read two registers
c) read the branch instruction
d) nothing or none of the above
Pipelined execution of a program

lw $t0, 4($sp)
sub $v0, $a0, $a1
and $t1, $t2, $t3
or $s0, $s1, $s2
add $t5, $t6, $s0

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Peer instruction

• How many instructions/cycle will MIPS processor achieve when pipelining and using each of the 5 stages (IF, ID, EX, MEM, WB) as a pipeline stage?

a) IPC = 5
b) IPC = 1/5
c) IPC = 1
d) IPC = 2
e) IPC < 1
Pipelined datapath
Peer Instruction

• How should we change the control unit to handle a pipelined processor (stages IF, ID, EX, MEM, WB)
  • single cycle control unit was some combinational logic

a) no change
b) implement as an FSM
c) calculate the control signals and pass them down the pipeline
d) a different control unit for each stage; pass the instruction bits down the pipeline
Next steps

• Next:
  • control for pipelined MIPS datapath
  • challenges with pipelining in a MIPS processor (hazards!)